REMARKS/ARGUMENTS

Claims 1-26 stand rejected in the outstanding Official Action. Claims 5 and 18 have been cancelled without prejudice and claims 1, 2, 14 and 15 have been amended. Accordingly, claims 1-4, 6-17 and 19-26 are the only claims remaining in this application.

In section 3, page 2 of the Official Action, the Examiner indicates that the Japanese Official Action previously filed with the Information Disclosure Statement has not been considered because the reference was not in English. Applicants enclose herewith an English translation to permit the Examiner's review of the Japanese Official Action thereby obviating any further objection.

In section 4 on page 2 of the Official Action, the specification is objected to as including a reference to Figure 7 in the Abstract. Applicants enclose an amended Abstract in which the reference to Figure 7 has been deleted, thereby obviating any further objection to the Abstract.

Claim 1 is objected to because claim 1 recites "store" in line 4 (presumably, it is line 4 although the line number is not recited in the official action) and in line 7 recites "saving." Applicants have amended claim 1, line 7 to delete "saving" and substitute --storing--, thereby obviating any further objections thereto.

In section 6, page 3 of the Official Action, claims 5 and 18 are objected to. Claims 5 and 18 have been cancelled without prejudice, thereby obviating any further objection thereto.

On page 3, section 8 of the Official Action, claims 1-26 stand rejected under 35 USC §112 (second paragraph) as allegedly being indefinite. Specifically, the Examiner suggests that in claim 1, lines 18 and 19, the recitation "determine stack priority level" is unclear. Applicants have amended independent claims 1 and 14 to indicate that the stack priority level is determined

when the stack data store is storing a plurality of sets of state data. This amendment precludes the interpretation taken by the Examiner (of the stack data store only storing the state data for a single interrupt when the stack priority level is determined).

On page 4, lines 1-5 of the Official Action, the Examiner questions not only the claim wording of "the stack priority level" (as discussed above), but "interrupt event priority" and "processing priority." Applicants have reviewed the claim language and can find no recitation of "interrupt event priority" or "processing priority." Where are these phrases used in the claims?

Additionally, as is well known to those of ordinary skill in the art, each interrupt event has an associated priority. The highest priority among all of the interrupt events for which state data is stored on the stack data store is the "stack priority level." This inherent aspect of a recited claim structure can clearly be referenced in the claim without *in haec verba* antecedent basis (MPEP §2173.05(e)).

As will also be understood by those of ordinary skill in the art, processing priority can be considered to correspond to the priority of the interrupt event currently being serviced, i.e., the interrupt event for which the interrupt handling code is currently executing. It should be noted that the stack data store stores state data corresponding to a plurality of interrupt events when these are nested interrupts. The existence of "nested interrupts" will be familiar to those of ordinary skill in the art and the ability of a stack data store to store one or more sets of state data also teaches the possibility of multiple nested interrupts. It is believed clear in Applicants' specification how multiple nested interrupts may arise and how these are handled in accordance with the present invention.

In any event, the above amendments to independent claims 1 and 14 are believed to obviate any remaining indefiniteness with respect to independent claims 1 and 14 or claims dependent thereon and any further rejection thereunder is respectfully traversed.

Beginning at section 10 on page 4 of the Official Action, the Examiner rejects claims 1-7, 10-12, 14-20 and 23-25 under 35 USC §103 as being unpatentable over Miu (U.S. Patent 4,488,227) in view of Ishimoto (U.S. Patent 5,410,715). Even though Miu is the primary reference, in the paragraph bridging pages 5 and 6, the Examiner admits that Miu "does not specifically disclose each interrupt is associated with a programmable priority level," that the "interrupt controller is further configured to determine a stack priority level corresponding to highest priority interrupt event among the interrupt events" and the interrupt controller is "further configured to detect that said one or more second interrupt events have a higher priority than said processing that was interrupted . . . ." These admissions that these positively recited claim elements and/or method steps are missing from the Miu reference are very much appreciated.

The Examiner states in the last two paragraphs on page 6 that the above features (admittedly missing from Miu) are somewhere disclosed in the Ishimoto reference. This is believed to be a completely unfounded allegation. Firstly, it should be clear that Ishimoto does not disclose determining any "stack priority level." While the Examiner suggests that column 1, lines 24-40 of Ishimoto disclose determination of stack priority level, this is incorrect and unsupported by the cited portion of the Ishimoto reference. Column 1, lines 24-40 of Ishimoto merely describes that an interrupt request can be acknowledged if its priority is higher than the priority of the interrupt request corresponding to the interrupt processing under execution. However, there is no disclosure of any "stack data store" in the Ishimoto reference. Therefore, it

could not disclose determining the highest priority interrupt event amongst interrupt events associated with the plurality of sets of state data stored in the stack data store.

There is simply nothing in column 1, lines 24-40 of the Ishimoto reference that discloses the claimed "stack data store" or the specifically claimed interrelationship of the interrupt controller with respect to determining a stack priority level in the manner specified in Applicants' independent claims, i.e., determining a stack priority level "corresponding to the highest priority interrupt event among said plurality of interrupt events associated with said plurality of sets of state data stored in said stack data store." Where or how the Examiner believes this to be disclosed in the Ishimoto reference is not apparent from the outstanding Official Action and clarification is respectfully requested.

On page 12 of the Official Action, the Examiner provides an "explanation" of his basis for rejecting independent claims 1 and 2 and argues that he has interpreted "stack priority level" as the "process or interrupt in service or the process that was interrupted with the first interrupt service is complete." This interpretation is incorrect and evidences the Examiner's failure to properly construe the claim. None of the processes noted by the Examiner are "corresponding to the highest priority interrupt event among said plurality of interrupt events associated with said plurality of sets of state data stored in said stack data store" so they quite clearly cannot disclose the claimed "stack priority level."

Because the Examiner fails to indicate where Ishimoto teaches a determination of "stack priority level" or the interrelationship of elements with such priority level as is set out in Applicants' independent claims, there is no disclosure of this claimed structure (or method step in claim 14) in the Miu/Ishimoto combination (especially since the Examiner admits this is

missing from Miu). Because the combination of elements does not disclose the claimed element, there can be no *prima facie* case of obviousness since the burden is on the Examiner to establish that the combination of prior art teaches all claimed elements. Accordingly, there is simply no support for the rejection of independent claims 1 and 14 or claims dependent thereon as obvious over the Miu/Ishimoto combination.

The Examiner also alleges that the claim requirement of "said interrupt controller is further configured to detect that said one or more second interrupt events have a higher priority than said processing that was interrupted by said first interrupt event if said one or more second interrupt event has a higher priority than said stack priority level" is disclosed in Ishimoto and this contention is also traversed. The Examiner suggests that this is somewhere disclosed in Ishimoto at column 4, lines 65-68 and column 5, lines 1-21. The above comments regarding the Examiner's admission that the "stack priority level" claimed element in claim 1 and method step in claim 14 is missing from the Miu and Ishimoto references are herein incorporated by reference. Because the Examiner admits that Miu does not contain this feature and because it has been shown that Ishimoto does not disclose the feature of "stack priority level," then Applicants' claimed feature of the interrupt controller which is based upon "stack priority level" cannot be disclosed or obvious in view thereof.

Further, even if Miu and Ishimoto are combined, they do not disclose the last two configurational aspects of the interrupt controller recited in Applicants' independent claim 1 or the method steps in independent claim 14. As a consequence, the Examiner fails to meet his burden of establishing a *prima facie* case of obviousness and any further rejection thereunder is respectfully traversed.

While it is clear that the language of Applicants' independent claims 1 and 14 is missing from any combination of the Miu and Ishimoto references, simple logic indicates that neither of these references have any recognition of the problem that is solved by Applicants' invention and therefore one would not look to these references to combine elements therefrom even if the claimed elements were somewhere disclosed in the references.

Neither Miu nor Ishimoto recognizes that priority levels associated with stacked interrupt events can be changed after the interrupt event occurs. It is noted that independent claims 1 and 14 have been amended to further recite in conjunction with the stack data store, that "each said interrupt event is associated with a priority that is programmable **both before and after** said interrupt event occurs" (emphasis added). Of course, since neither Miu nor Ishimoto teaches the determination of a "stack priority level," it is doubtful that there is any disclosure of a "priority that is programmable both before and after said interrupt event occurs" as required in the claims.

As a result, neither Miu nor Ishimoto could recognize the problem that occurs when a stacked interrupt has its priority changed to a higher priority than the interrupt at the top of the stack. Applicants note that the above argument as to patentability over the Miu/Ishimoto combination was previously made to the Examiner, who responded in section 36 on page 12 by arguing that the feature of altering priority levels was not included in the claims. Although Applicants note that it was inherently included in the operational interrelationship of the elements of the claims as originally proposed, it is now specifically recited in the claims.

Accordingly, this feature of the claims is not recognized by the Miu and Ishimoto references and consequently the problem of priority changing is not addressed and it would

certainly not be obvious to solve the problem in the manner of Applicants' independent claims 1 and 14.

In view of the above, the Examiner has failed to properly support his rejection of independent claims 1 and 14 and claims dependent thereon over the Miu/Ishimoto combination and any further rejection thereunder is respectfully traversed.

Claims 8, 9, 21 and 22 stand rejected under 35 USC §103 as unpatentable over Miu/Ishimoto in view of McMahan (U.S. Patent 5,706,491). Claims 8, 9, 21 and 22 ultimately depend from claims 1 and 14 and therefore the above comments regarding claims 1 and 14 and the impropriety of the rejection over the Miu/Ishimoto combination are herein incorporated by reference.

It is also noted that in the rejection of claims 8, 9, 21 and 22, the Examiner does not allege that the McMahan reference discloses any of the features admitted by the Examiner or identified by Applicant to be missing from the Miu and Ishimoto combination (as noted above). Accordingly, even if Miu, Ishimoto and McMahan were combined as suggested by the Examiner, all claimed features of the independent claims would still be missing and therefore the Examiner would not have met his burden of establishing a *prima facie* case of obviousness. As a result, any further rejection of claims 8, 9, 21 and 22 under 35 USC §103 is respectfully traversed.

Claims 13 and 26 stand rejected under 35 USC §103 as unpatentable over Miu/Ishimoto in view of Raasch (U.S. Patent 5,237692). Claims 13 and 26 depend from claims 1 and 14 and therefore the above comments regarding claims 1 and 14 and the impropriety of the rejection over the Miu/Ishimoto combination are herein incorporated by reference.

It is also noted that in the rejection of claims 13 and 26, the Examiner does not allege that the Raasch reference discloses any of the features admitted by the Examiner or identified by the Applicant to be missing from the Miu and Ishimoto combination (as noted above). Accordingly, even if Miu, Ishimoto and Raasch were combined as suggested by the Examiner, all claimed features of the independent claims would still be missing and therefore the Examiner would not have met his burden of establishing a *prima facie* case of obviousness. As a result, any further rejection of claims 13 and 26 under 35 USC §103 is respectfully traversed.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that remaining claims 1-4, 6-17 and 19-26 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicants' undersigned representative.

Respectfully submitted,

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Attachment:
English translation of JP Office Action

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Ref. No. PA-31728EY

Mailing No. 754414
Mailing Date: December 9, 2008

Translation of Official Action

Japanese Patent Appln. No. 2004-367705
Date of Issued: December 5, 2008
Name of Examiner: Masaya Tonokawa
Patent Attorney: Kiyoshi Asamura and three others
Article Applied: Patent Law Articles 36, 29.(2)

This application should be rejected for the reasons given below. In response, the applicant may file an Argument and/or Amendment within three months from the mailing date.

Reason 1

This application does not satisfy the requirements prescribed in Article 36 of the Patent Law in the following respects:

Reason 2

The invention(s) of the claim(s) is considered to be readily thought of from the disclosure in the undermentioned publication circulated in Japan or in foreign countries prior to the filing of this application. Therefore, this application falls under the provisions of Article 29.(2) of the Patent Law and thus is not acceptable.

Remarks

[REASON 1]

[Cited Reference List]

1. JP-B2-H6-66051 (Patent Family US4,488,227)
2. US5,706,491
3. US5,237,692

[CLAIMS] 3,6,8-11,16,19,21-24

a) Claim 3 includes "said processing being performed when said first interrupt event occurred". It is unclear which part of claim 1 corresponds to "said processing". (Does it means "redirect program instruction execution to a first interrupt handling program" or both of "save to a stack data store" and "redirect program instruction execution"?)

b) Claim 3 includes "execution of a non-interrupt triggered program". The term "non-interrupt trigger" is not a well-known term. It is unclear which kind of technical matter it specifies even if the specification is referred to.

c) (We can handle the matter without your assistance.)

Claim 16 includes the same problems mentioned in a) to c).

d) Claim 6 includes "a late interrupt signal". The term "late" is unclear in its standard and its degree and the technical contents to be specified is unclear. Claim 19 includes the
similar problem.

Claims 8-9 and 21-22 depending from claims 6 and 19 are also unclear.

e) Claims 9 and 11 include "link register" and "link address", which technical contents to be specified are unclear.

Claims 22 and 24 have the same problem.

f) Claim 10 describes "transfer of data values to said stack data store under control of said interrupt controller is performed in parallel with and asynchronously to loading

of program counter location and program instructions into an instruction pipeline prior to execution". It appears to specify an object by function. However, the concrete object can not be assumed and it is unclear which kind of object is specified even if the specification is referred to.

Claim 23 includes the same problem.

Accordingly, the invention relating to claims 3,6,8-11,16,19 and 21-24 is not clear.

Remarks

[REASON 2]
[CLAIMS] 1-7, 10-12, 14-20 and 23-25
[Cited Reference] 1
[Note]

Reference 1 relates to the service process of the nested interrupts in a data processor. It discloses to control the last-in first-out stack not to perform any fetch operation or any push operation ("without saving further state data to said stack data store" of the present invention) if any interrupt occurs ("if such a said one or more second interrupt events has occurred") when returning from the interrupt service routine ("upon completion of said first interrupt handling program")in page 4, right column, line 43 to page 5, left column, line 1 (corresponding to "OBJECT OF THE INVENTION" and "SUMMARY OF THE INVENTION" in columns 3 and 4 of US4,488,227).

It is normally performed that the execution of the high priority interrupt handling program is given priority over the execution of the low priority interrupt handling program.

Accordingly, the invention relating to claims 1-7, 10-12, 14-20 and 23-25 can be easily thought of by those skilled in the art based on the invention described in Reference 1.

[CLAIMS] 8-9 and 21-22
[Cited References] 1 and 2
[Note]

Reference 2 discloses to repair the return stack pointer in the branch control unit of the processor (in mainly column 3, line 54 to column 4, line 20).

Accordingly, the invention relating to claims 8-9, 21-22 can be easily thought of by those skilled in the art based on the inventions described in References 1 and 2.

[CLAIMS] 13 and 26
[Cited References] 1 and 3
[Note]

Reference 3 discloses the interrupt controller which operates in a low power mode while awaiting interrupts (in mainly column 2, line 63 to column 3, line 4).

Accordingly, the invention relating to claims 13 and 26 can be easily thought of by those skilled in the art based on the inventions described in References 1 and 3.

Other reason for rejection will be notified if new reason is found.

Record of Prior Art Searched

Technical Field Searched: IPC G06F9/22-9/28

The record of Prior Art Searched does not constitute any reason for rejecting this application.